A Solid State Current Limiter

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EPRI's Solid State Current Limiter

Long an objective

New factors to consider:

Constantly decreasing component costs

Technical effects of deregulation -

Merchant plants may locate at sites that increase available fault currents

Loss evaluation less of a factor

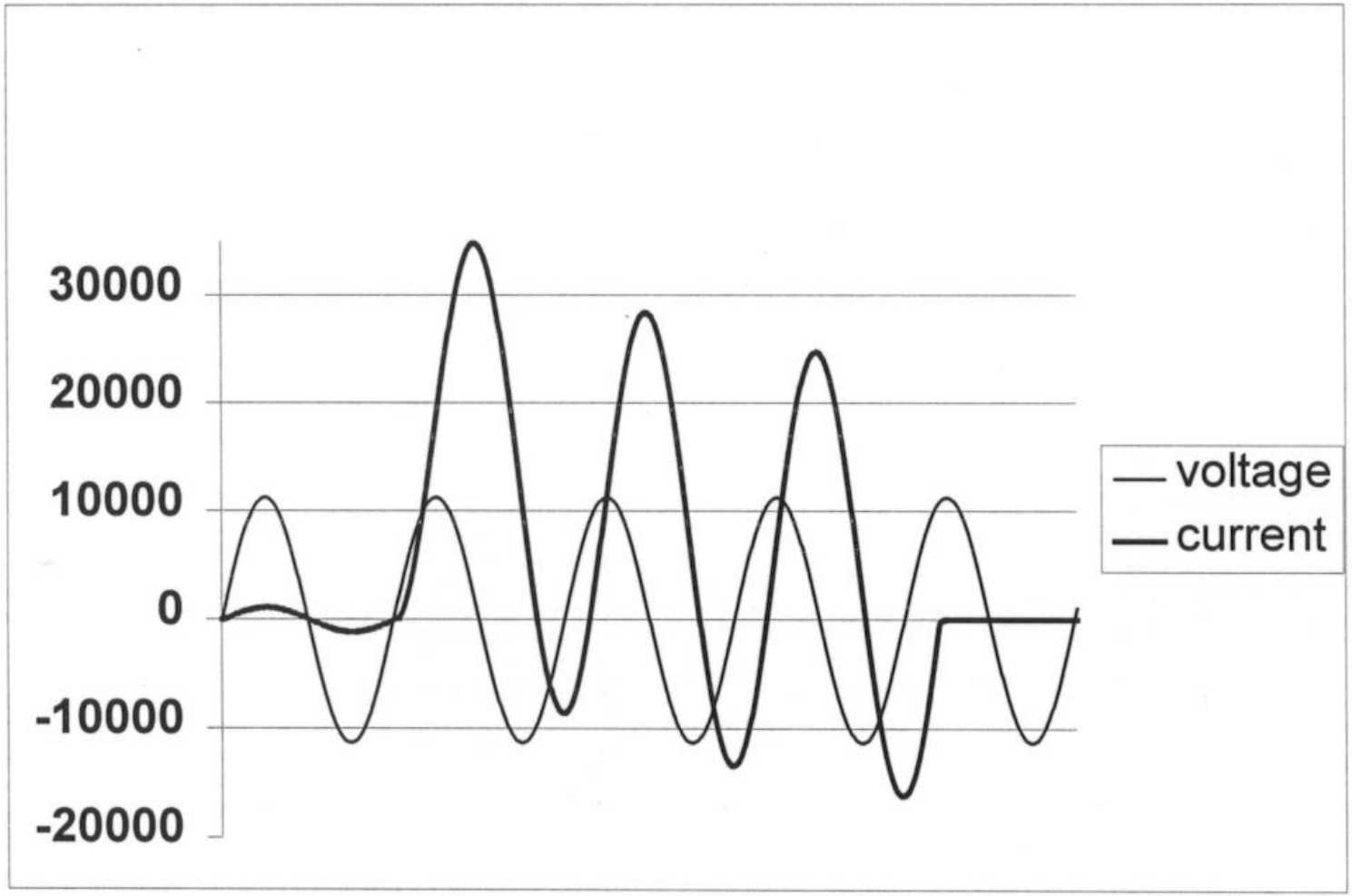
Solid State Current Limiter

Strategy:

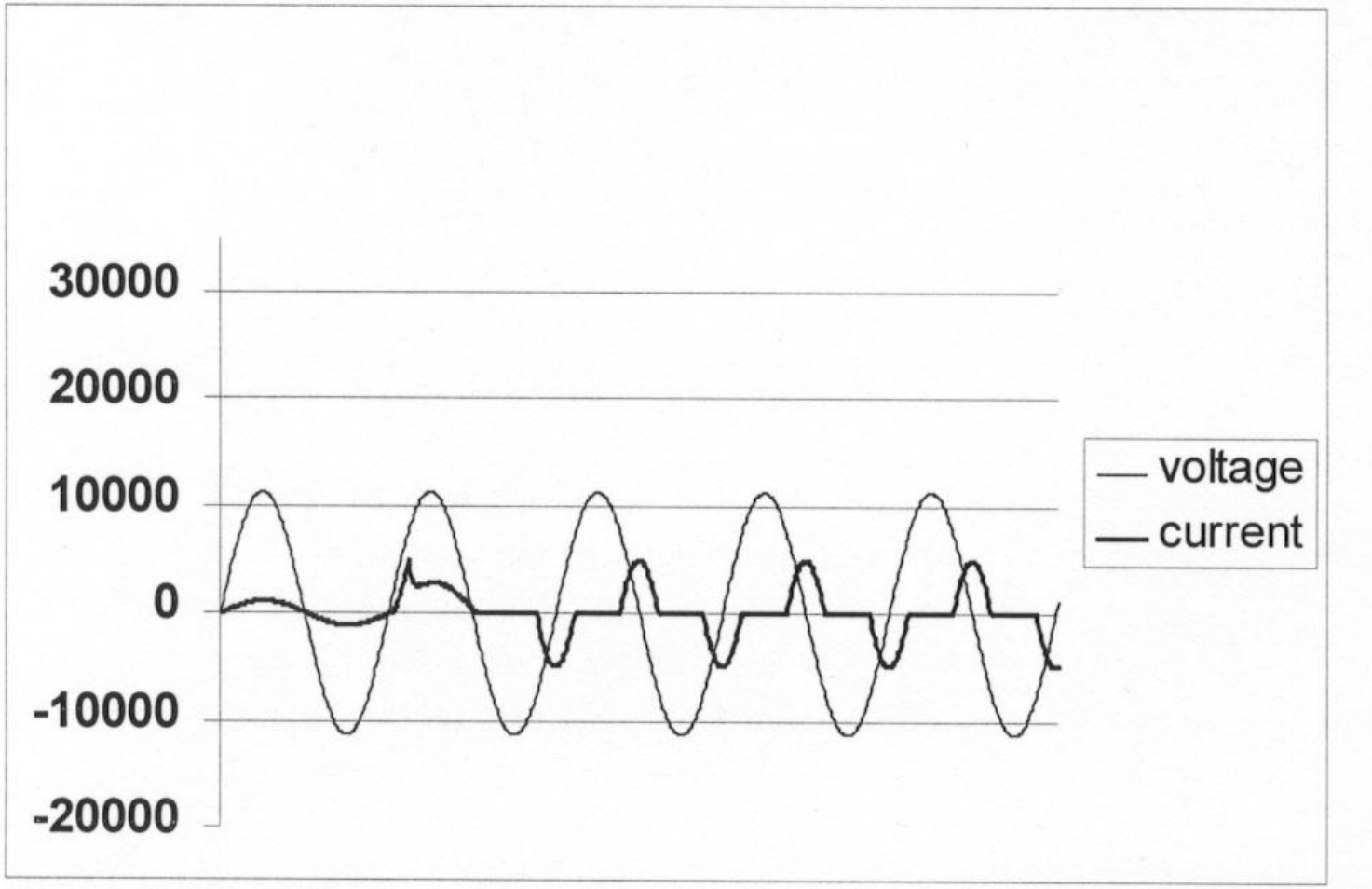
Develop module that can be stacked for different voltage ratings

Begin field trials at distribution voltages, move to transmission after some experience

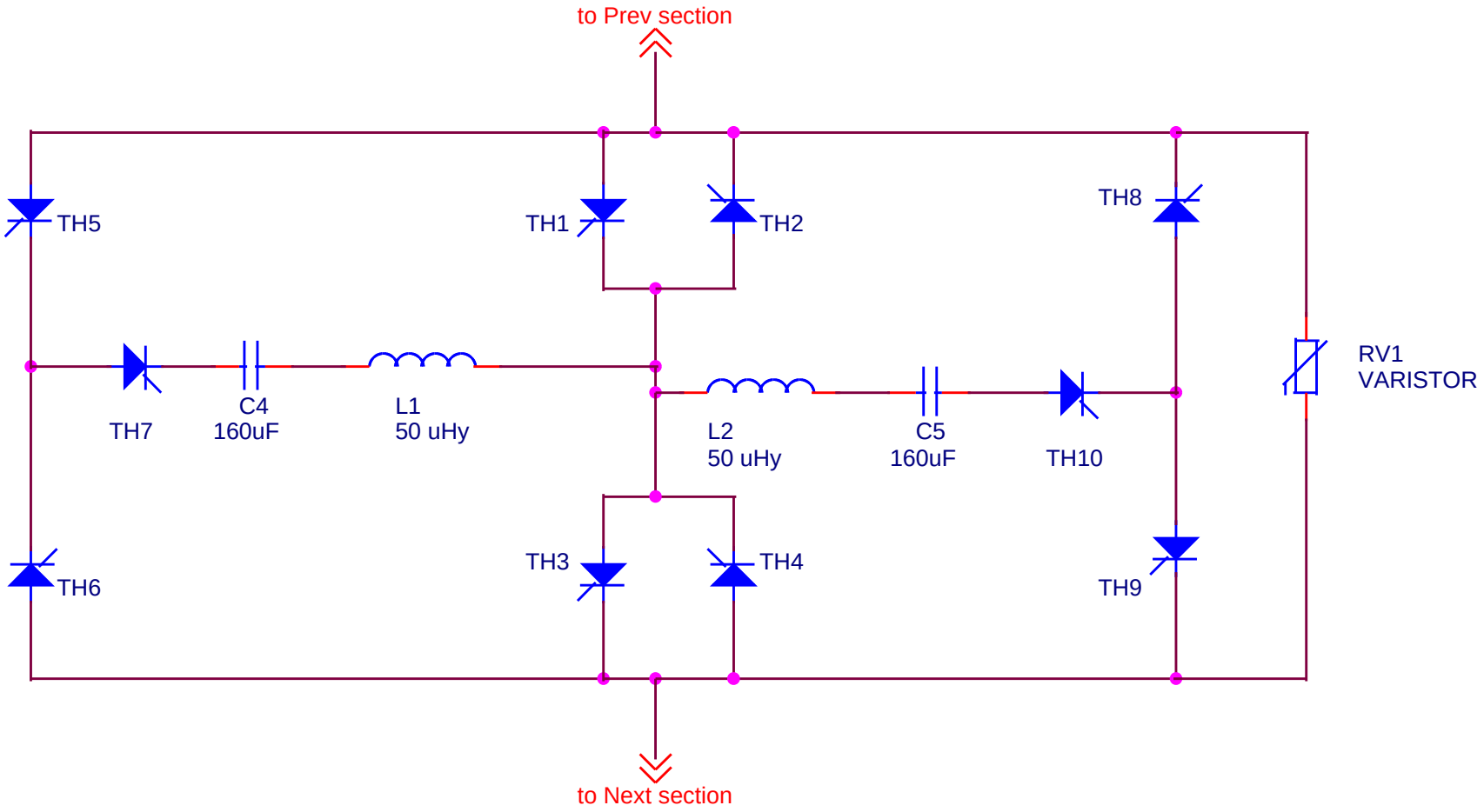
Single Line to Ground Fault Conventional Breaker



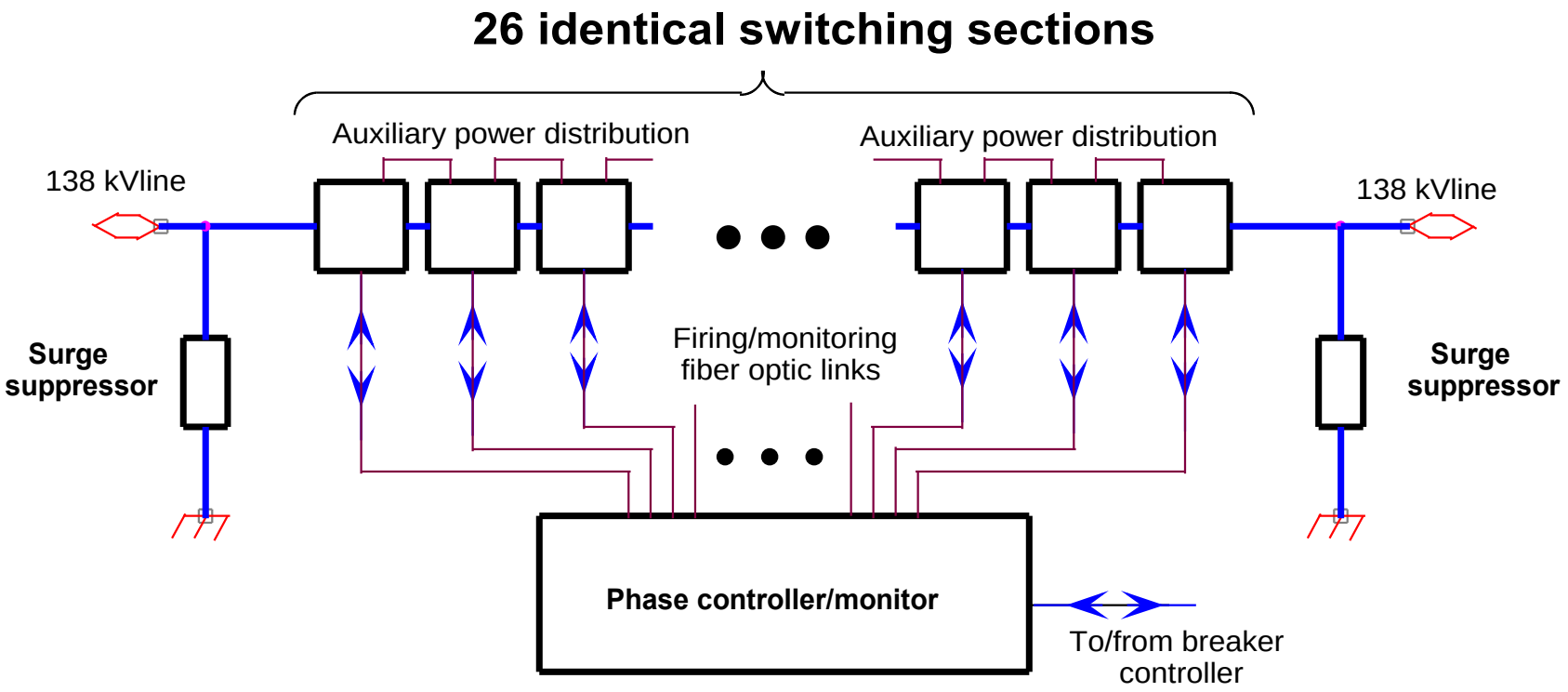
Single Line to Ground Fault
SSCL with Current Limiting



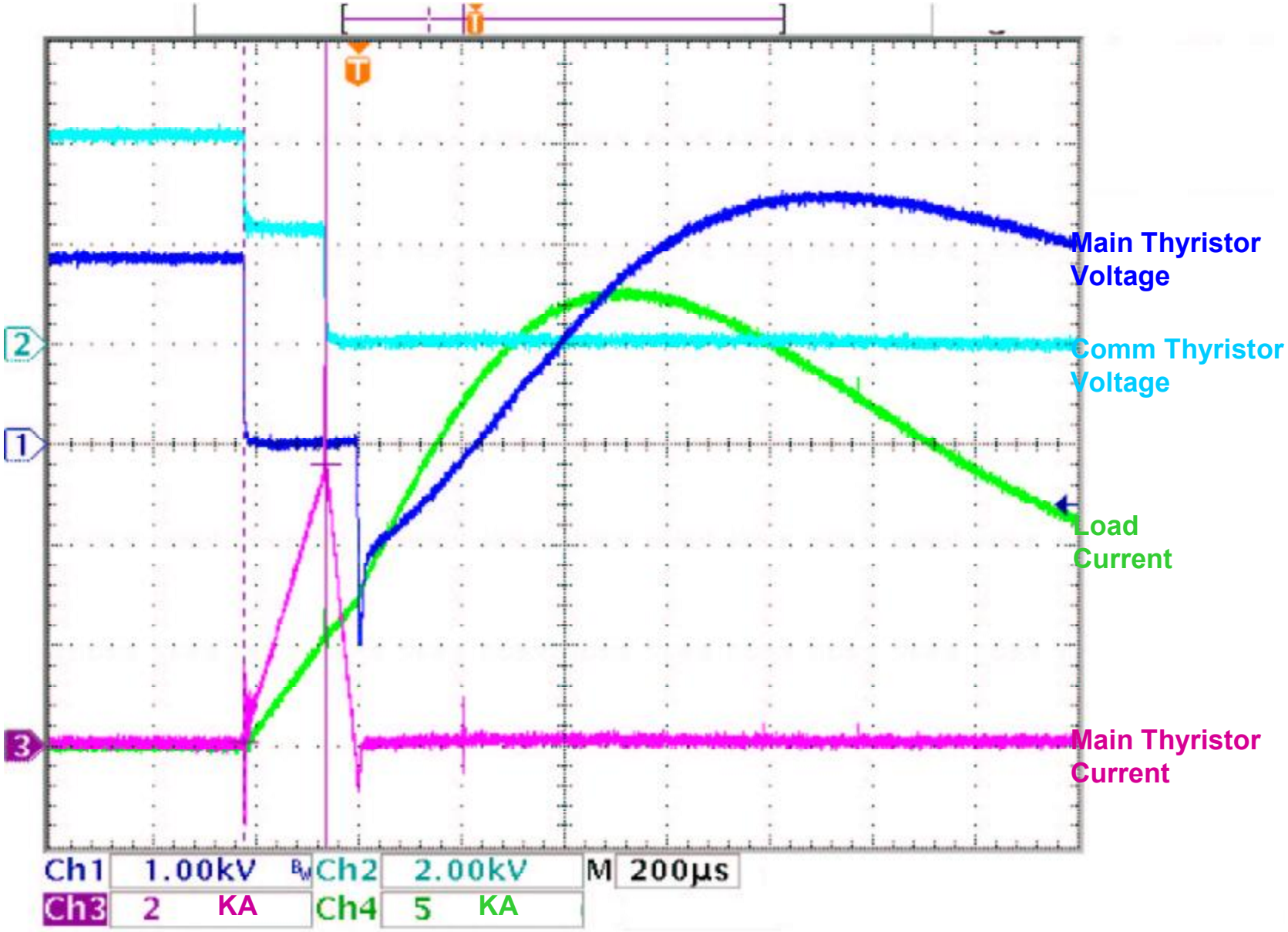
Thyristor module
5000 V each, 2 in series



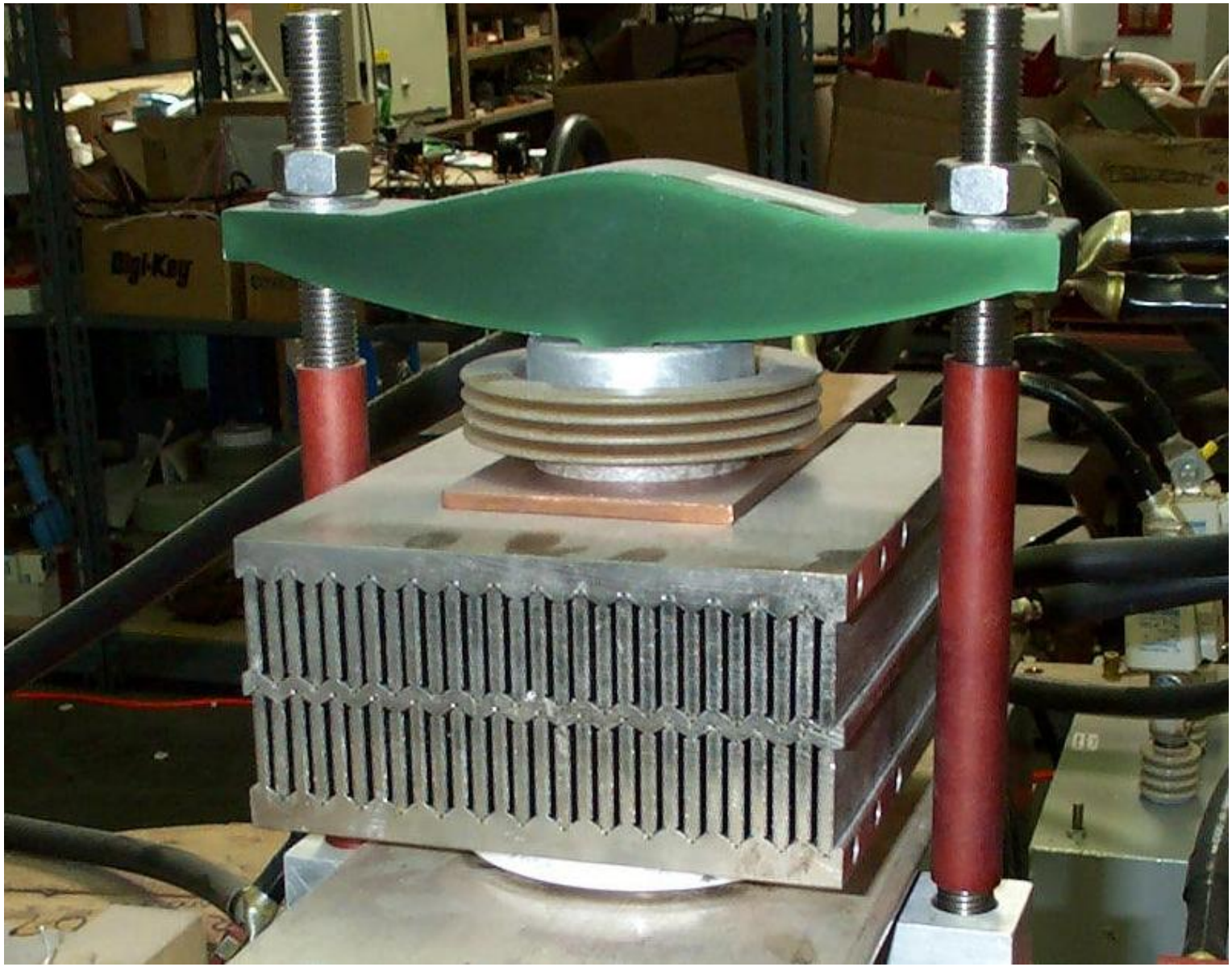
Overall Structure of SSCL

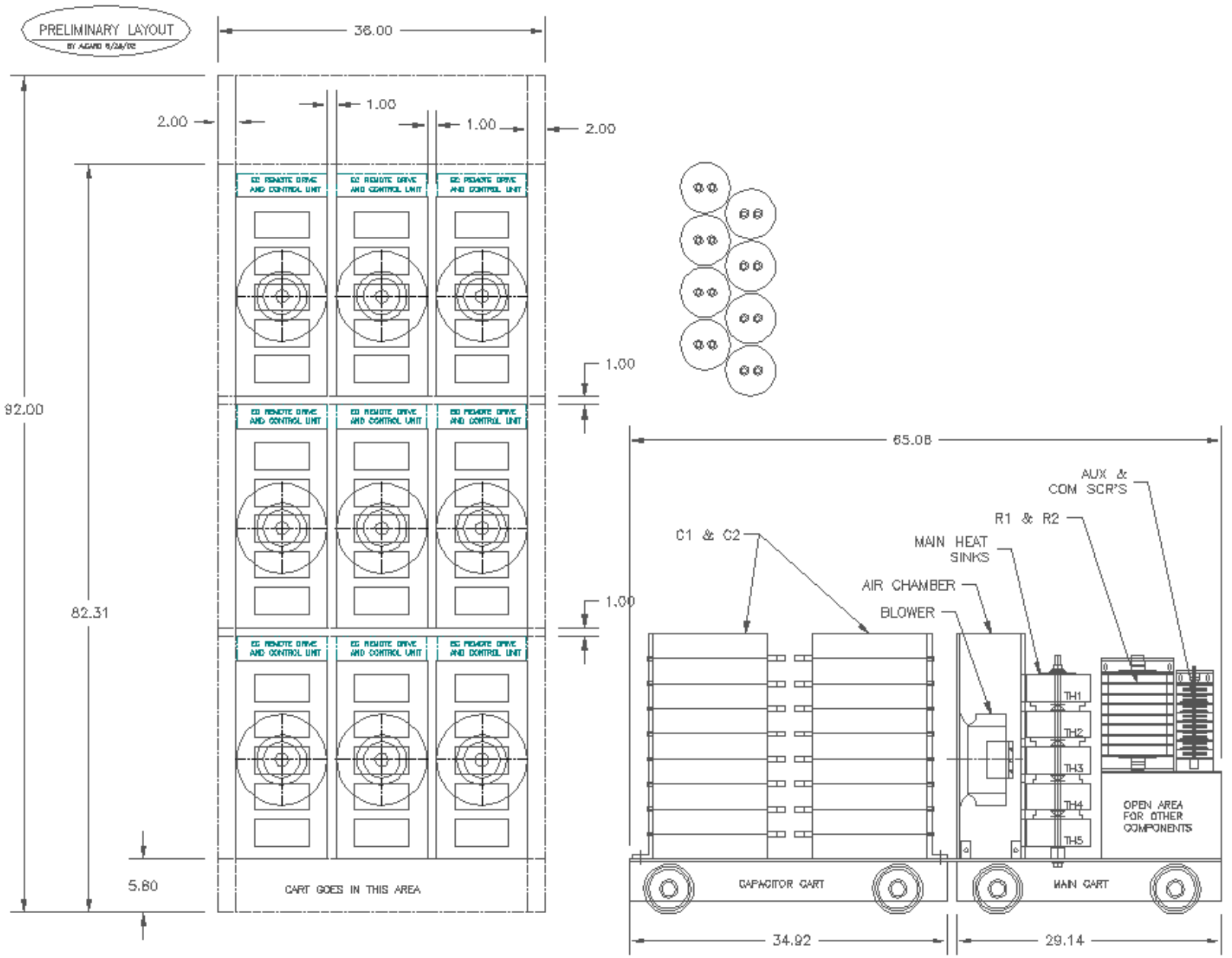



DANGER


Main Thyristor Voltage
Comm Thyristor Voltage
Load Current
Main Thyristor Current
2
1
3
Ch1 1.00kV
Ch2 2.00kV
M 200µs
Ch3 2 KA
Ch4 5 KA


WESTCODE
WESTCODE
WESTCODE


Digi-Key


PRELIMINARY LAYOUT
BY AGARD 6/26/02
36.00
2.00
1.00
1.00
2.00
92.00
82.31
1.00
1.00
5.80
CART GOES IN THIS AREA
65.08
AUX &
COM SCR'S
R1 & R2
C1 & C2
MAIN HEAT
SINKS
AIR CHAMBER
BLOWER
TH1
TH2
TH3
TH4
TH5
OPEN AREA
FOR OTHER
COMPONENTS
CAPACITOR CART
MAIN CART
34.92
29.14

Solid State Current Limiter

Advantages compensate for higher costs:

One current limiter can extend the usefulness of many conventional breakers

Reliability and life -

Reduced current and voltage peaks seen by other equipment

Power quality improved

Solid State Current Limiter

Applications:

Tie breaker position to limit fault current

Minimize switching transient on transmission line

Capacitor bank switching at frequent intervals

Improved power quality for customer; fire hazard case as example

Solid State Current Limiter

Funding and Hosting:

Development phase to be covered by EPRI funds

Extra funds from utilities are speeding the work

Looking for host utilities for field trials in 2003

of medium voltage device

Solid State Current Limiter

Nomenclature dictated by standards

Because we will have slightly different specifications, we will call this device a “current limiter” and not a “circuit breaker.”

EPRI's Post Silicon Initiative

- SiC and GaN have potential for higher voltage and higher temperature
- Can we make further big steps in Si?
- This work funded by Strategic Science and Technology at EPRI

EPRI's Post Silicon Initiative

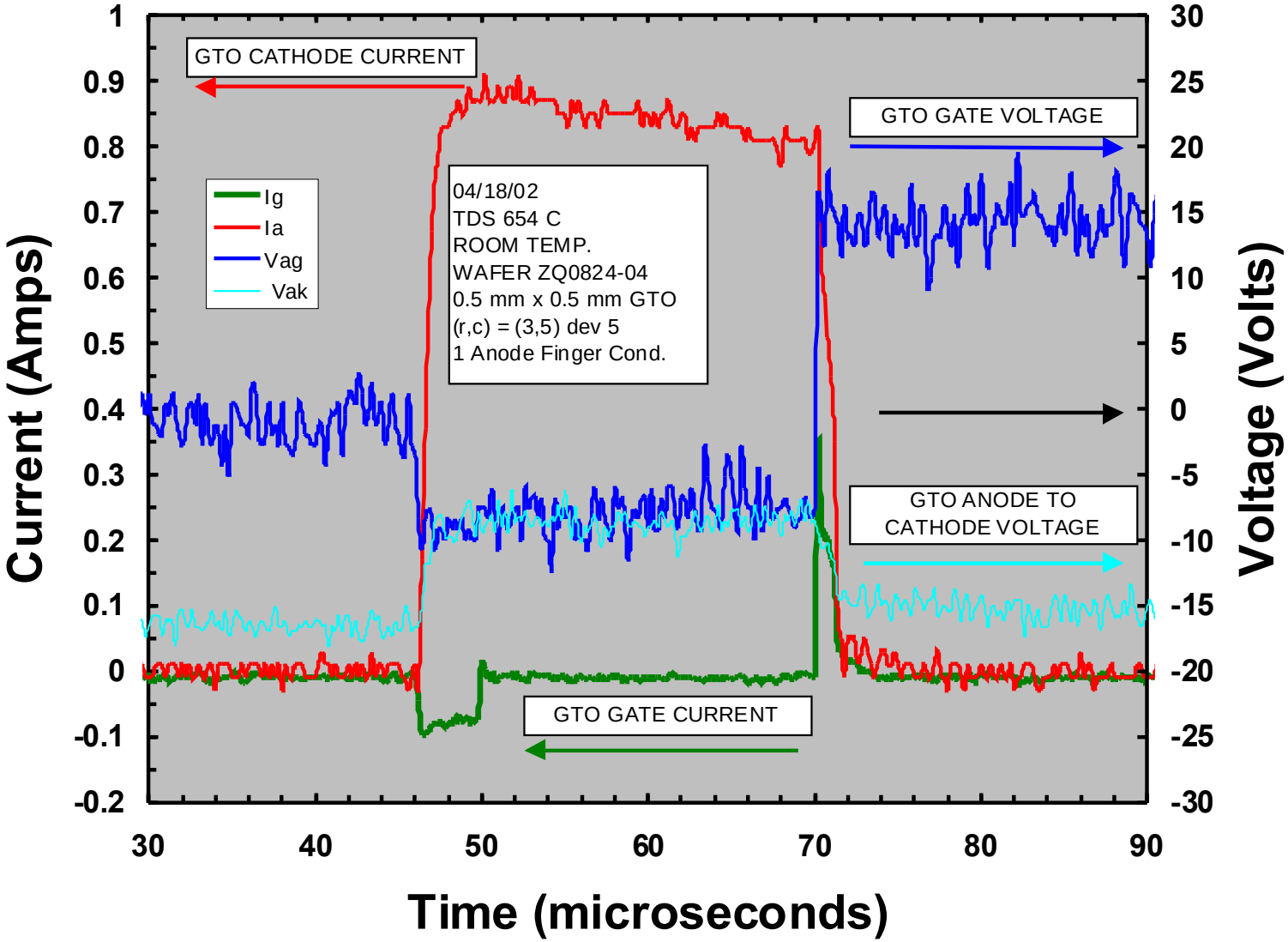
SiC GTO

Higher than 6 kV blocking

Operating temperature above 250 C

Thermally advanced packaging for parallel operation

SiC GTO: 0.5 mm sq. rated 5 kV



EPRI's Post Silicon Initiative

Si "Super" GTO

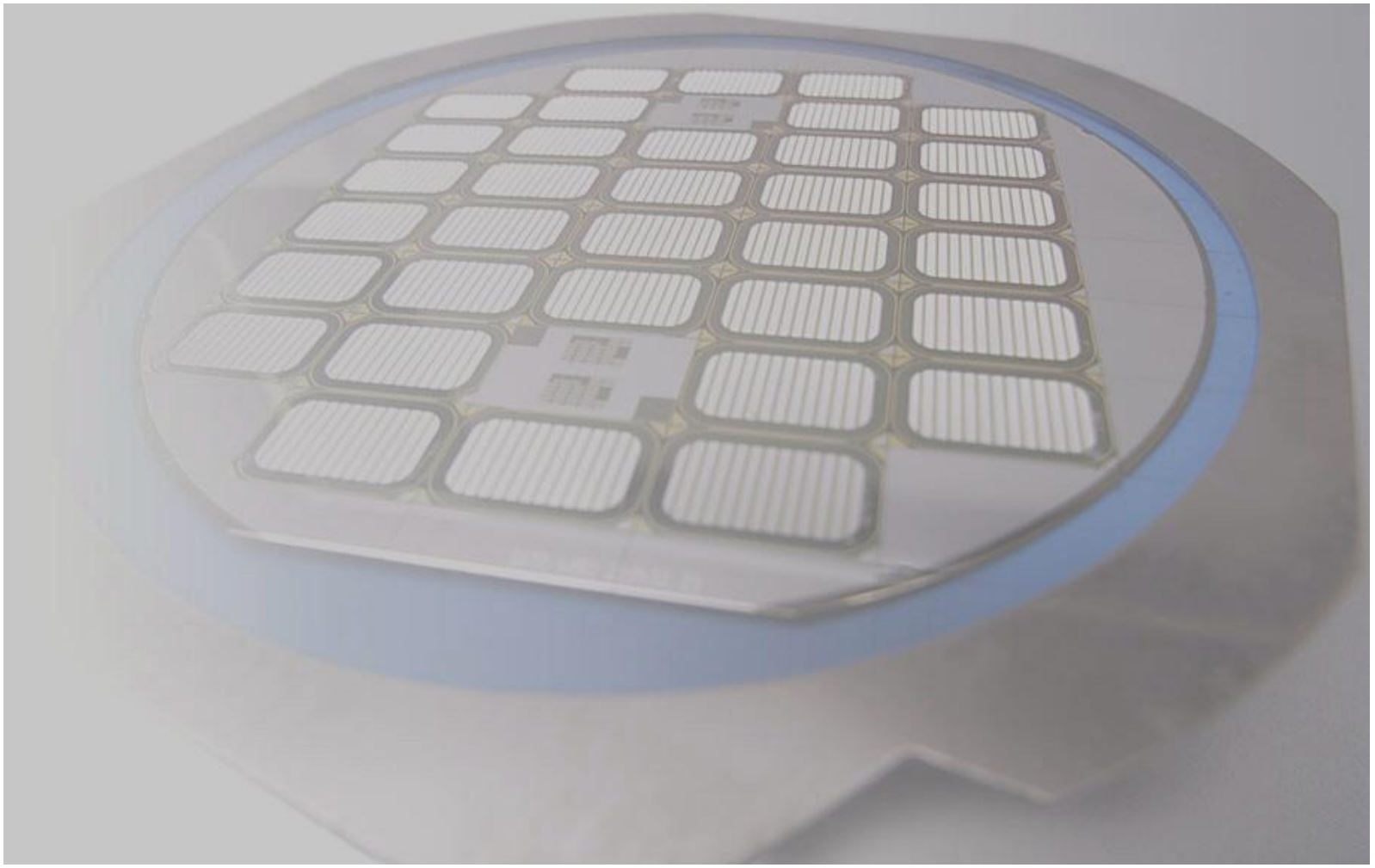
Higher than 5 kV blocking

Higher turn off current density

Faster speed

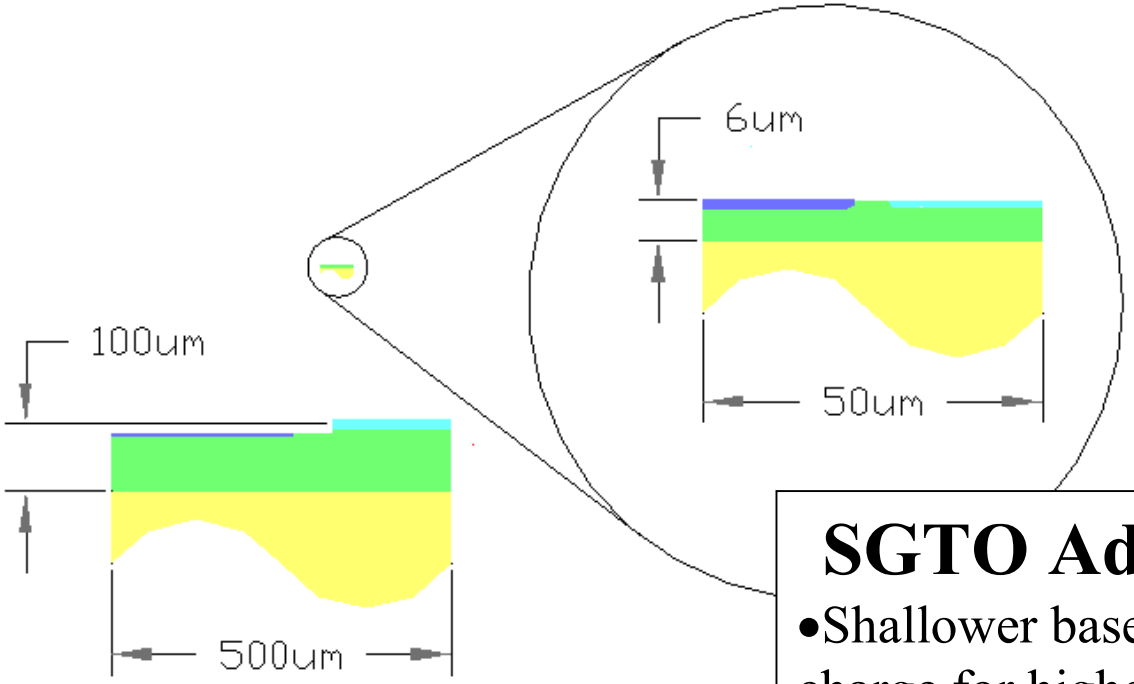
Smaller gate power

1 x 2 cm size



Silicon wafer with SuperGTOs

SuperGTO vs. Standard GTO



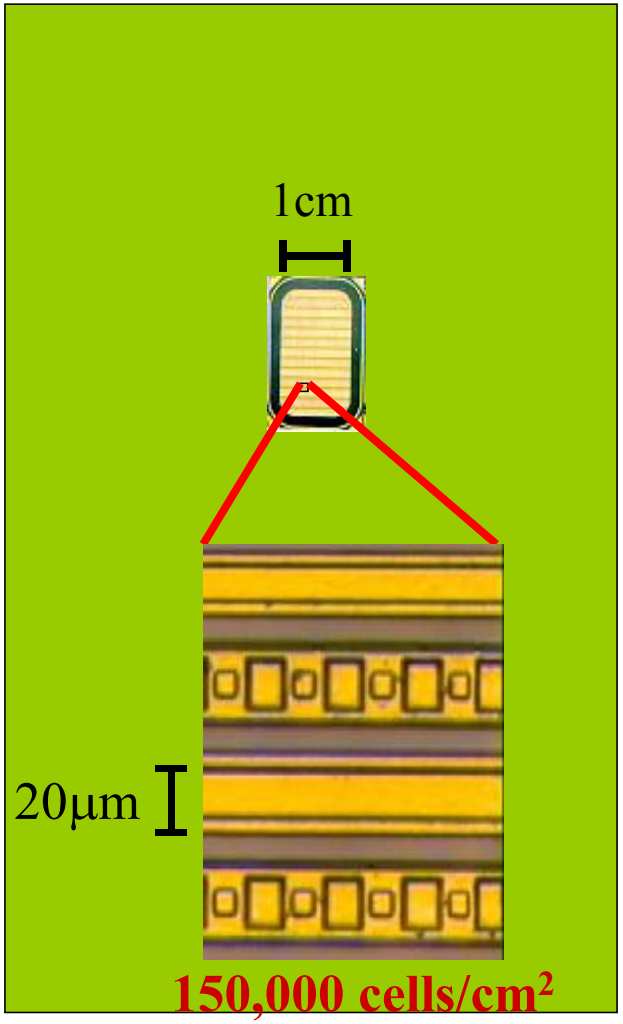
Super GTO
Upper Base Region
Q ~ 2 e13/cm^2

Standard GTO Upper Base Region
Q ~ 1.2 e14/cm^2

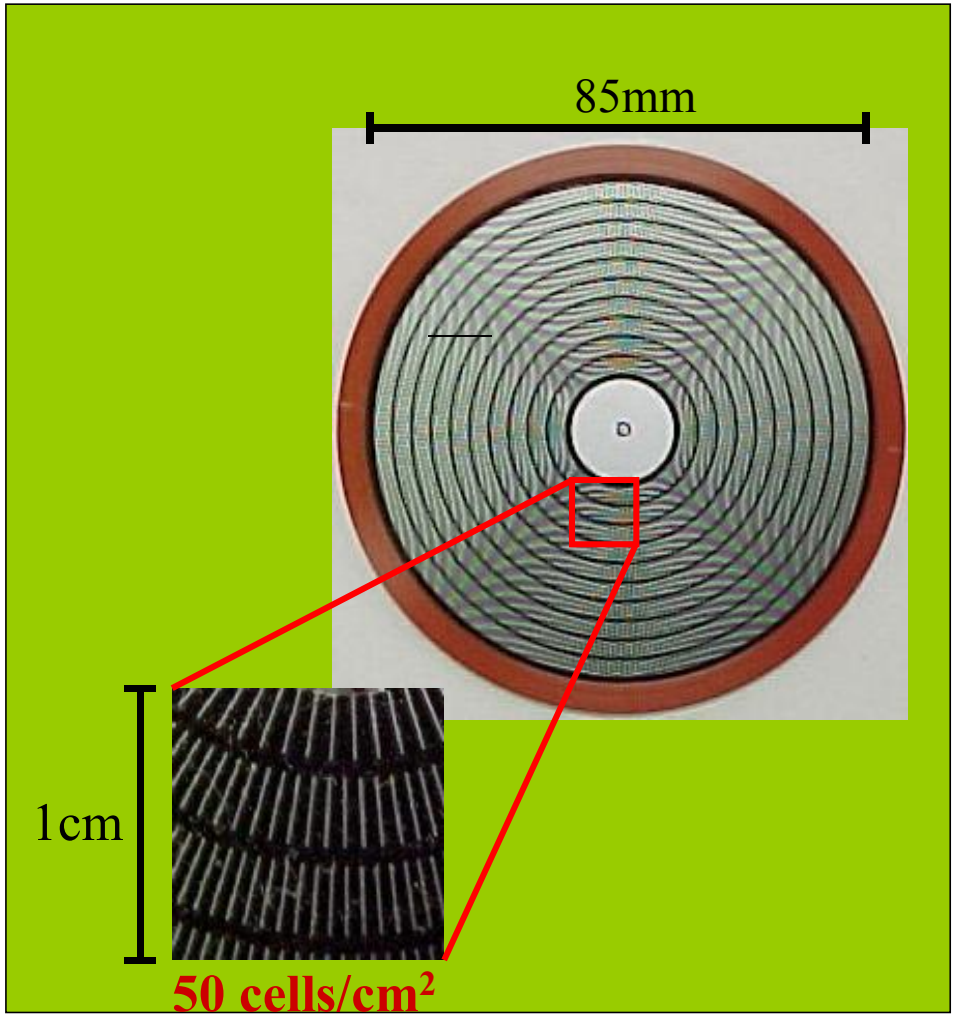
SGTO Advantage

- Shallower base with less charge for higher speed and lower forward drop.
- Narrower cell for 10x higher turn-off capability.

Super GTO



Standard GTO



3,000 x in cell density gives 10x increase in turn-off current density.